UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/824,008	04/14/2004	Shuo-Hsiu Hu	AUO-102	5926

7590 03/22/2007

David I. Roche
BAKER & McKENZIE
130 E. Randolph Drive
Chicago, IL 60601

EXAMINER	
SHENG, TOM V	
ART UNIT	PAPER NUMBER
2629	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/22/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/824,008	HU ET AL.	
	Examiner	Art Unit	
	Tom V. Sheng	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4/19/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-8, 15-20 and 22-25 are rejected under 35 U.S.C. 102(e) as being anticipated by Asano et al. (US 6,768,482 B2), hereinafter Asano.

As for claims 1 and 7, Asano teaches an electroluminescent display (fig. 3) comprising:

at least one scan line (scanning lines 12_i to 12_{i+2}; column 4, lines 23-34);

a plurality of data lines (data lines 13_i to 13_{i+2}; column 4, lines 23-34);

a plurality of light-emitting devices (organic EL device EL_{ii}; column 4, lines 35-41); and

a plurality of electrical addressing devices respectively coupling each of the light-emitting devices to one data line and the at least one scan line (each device EL_{ii} is controlled by a selection transistor TR_{iia} and a driving transistor TR_{iib} connecting to a respective gate line and data line; column 4, lines 42-59);

wherein the light-emitting devices include display areas (light emitting regions of sub-pixels; fig. 6A) arranged according to a non-uniform distribution along the at least

one scan line (the R, G, B sub-pixels are in a delta arrangement while sub-pixel circuits in fig. 6B are in a stripe arrangement; as shown, the R, G, B sub-pixels are arranged non-uniformly along respective horizontal/scanning lines; column 5, lines 40-62). Fig. 6C shows how the two arrangements are overlapped.

As for claims 2 and 16, the sub-pixels R and B are shown (fig. 6A) being offset from adjacent sub-pixel G (of the same pixel) in a direction substantially perpendicular to the scanning line.

As for claims 3 and 17, the sub-pixels R and G (alternatively B and G) of each pixel are at different levels.

As for claims 4-5 and 18-19, Asano teaches a modification (fig. 14) where a scan line is crenelated and with increased light emitting regions located alternately at two sides of the scan line (column 8, line 56 through column 9, line 34).

As for claim 6, Asano teaches that each device EL_{ij} is an organic EL device, which is also known as an organic light-emitting diode. For evidence, see column 1, lines 34-36 of Lee (US 6,741,037 B2).

As for claims 8 and 24, each selection transistor TR_{ija} is connected between a corresponding gate line via its gate and a data line via its drain, and a driving transistor TR_{ijb} is connected to corresponding selection transistor TR_{ija} via its gate. When active, current flows from power supply line 14 through the device EL_{ij} to ground 15 (column 4, lines 50-60). It is inherent that addressing comes from gate lines and image signals come from data lines.

Claim 15 is rejected per analysis of claim 1 and further with each pixel having respective R, G and B sub-pixels.

As for claim 20, the cathode of each device EL_{ii} of a sub-pixel corresponds to claimed display electrode.

As for claim 22, each sub-pixel does have a corresponding device EL_{ii} (light-emitting device) coupled to a selection transistor TR_{iia} and a driving transistor TR_{iib} (electrical addressing device).

As for claim 23, the selection transistor TR_{iia} is a switch thin film transistor and the driving transistor TR_{iib} is a driver thin film transistor.

As for claim 25, the R, G and B sub-pixels of each pixel are arranged in a delta configuration as shown in fig. 6A.

3. Claims 9-11, 14-17, 20, 21 and 25 are rejected under 35 U.S.C. 102(e) as being anticipated by Hong et al. (US 6,833,890 B2), hereinafter Hong.

As for claim 9, Hong teaches a liquid crystal display (fig. 6, 7) comprising:

at least one scan line (scanning lines 221 and 222; column 8, lines 10-14);

a plurality of data lines (data lines 62R, 62B1, 62G, 62R, 62B2 and 62G; column 8, lines 10-14);

a plurality of display electrodes (pixel electrodes 82R, 82B1, 82G, 82R, 82B2 and 82G; column 8, lines 14-18); and

a plurality of electrical addressing devices (thin film transistors as shown at respective pixels R, B1, G, R, B2 and G; column 8, lines 24-29) respectively coupling

each display electrode to one data line (for example, pixel electrode 82R is coupled to data line 62R via a source electrode 65) and the at least one scan line (via a gate electrode 26);

wherein the display electrodes are arranged according to a non-uniform distribution along the at least one scan line (as shown, the pixel electrodes disposed along scanning line 221 or 222 are non-uniform in shape).

As for claims 10 and 16, the pixel electrodes 82B1 or 82B2 is shown (fig. 6) being offset from adjacent pixel electrodes 82R and 82G in direction substantially perpendicular to the scan line 221 or 222.

As for claims 11 and 17, the pixel electrodes 82R and 82B1 are at different levels from each other and thus read on claimed at least a first display area and a second display area having different leveled portions.

As for claims 14 and 21, thin film transistors each including a gate electrode 26 that connects to gate lines 221 or 222, a source electrode 65 that connects to a data line (e.g. 62R), and a drain electrode 66 that connects to a pixel electrode (e.g. R) correspond to claimed gate terminal connected to at least one scan line, a drain terminal connected to one data line, and a source terminal connected to one display electrode. See fig. 6 and column 8, lines 24-29.

Claim 15 is rejected per analysis of claim 9 and further with each pixel having sub-pixels R, B1, G or R, B2, G.

As for claim 20, the sub-pixels R, B1, G, R, B2, G include pixel electrodes 82R, 82B1, 82G, 82R, 82B2 controlled by respective thin film transistors.

As for claim 25, the R, B1, G, R, B2, G sub-pixels of respective pixels are arranged in a delta configuration as shown in fig. 6.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hong as applied to claim 9 above, and further in view of Asano.

As for claims 12-13, Hong's gate line 221 or 222 is straight and thus does not teach a scan line with a crenelated profile. On the other hand, Asano teaches a modification (fig. 14) where a scan line is crenelated and with increased light emitting regions located alternately at two sides of the scan line (column 8, line 56 through column 9, line 34). One of ordinary skill in the art would recognize that using a crenelated scan line profile would advantageously increase Hong's color sub-pixel size.

Therefore, it would have been obvious to incorporate a crenelated gate line naturally with color sub-pixels distributed alternately along both sides of the gate line because of the advantage of having a larger sub-pixel size for display.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tom V. Sheng whose telephone number is (571) 272-7684. The examiner can normally be reached on 9:00am - 6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Tom Sheng

AMR A. AWAD
SUPERVISORY PATENT EXAMINER